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	Filing Date		2006-09-28	
	First Named Inventor	Monferrer, Pedro Chaparro		
	Art Unit	2115		
	Examiner Name	TRAN, VINCENT HUY		
	Attorney Docket Number	P23882		

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1	UNSAI, et al., "Impact of Parameter Variations on Circuits and Microarchitecture", IEEE Micro, vol.26(6), Nov.-Dec. 2006, pp. 30-39, total 11 pages	<input type="checkbox"/>
2	UHT, AUGUSTUS K., "Achieving Typical Delays in Synchronous Systems via Timing Error Tolerantion", University of Rhode Island, Dept. of Electrical Computer Engineering Technical Report No. 032000-0100, March 10, 2000, 21 Pages.	<input type="checkbox"/>
3	Office Action received for U.S. Patent Application No. 11/361,767, mailed on July 30, 2009, 16 pages.	<input type="checkbox"/>
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